

[Signature]

What is claimed is:

- 1 1 A method comprising:
2 receiving a request from a first computer system for identification of a second
3 computer system;
4 retrieving an identifier that identifies the second computer system;
5 encrypting the identifier with a key associated with the first computer system to
6 produce a hash value; and
7 providing the hash value to the first computer system in response to the request.

- 1 2. The method of claim 1, wherein the act of retrieving the identifier
2 comprises:
3 retrieving a processor number that identifies a processor of the second computer
4 system.

- 1 3. The method of claim 2, further comprising:
2 executing a processor instruction; and
3 retrieving the number in response to the execution of the instruction.

- 1 4. The method of claim 1, further comprising:
2 receiving the key from the first computer system.

- 1 5. The method of claim 1, wherein the key indicates an address of a web site.

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1 6. A computer system comprising:
2 an interface adapted to:
3 receive a request from another computer system for identification of the _____
4 first computer system, and
5 furnish a hash value that identifies the first computer system to said
6 another computer system; and
7 a processor coupled to the interface and adapted to:
8 encrypt an identifier that identifies the first computer system with a key
9 associated with said another computer system to produce the hash value.

1 7. The computer system of claim 6, wherein the identifier comprises a
2 processor number that identifies the processor.

1 8. The computer system of claim 6, wherein the processor comprises:
2 a memory adapted to store microcode for performing the encryption; and
3 a control unit coupled to the memory and adapted to execute the microcode to
4 perform the encryption.

1 9. The computer system of claim 6, wherein the processor is further adapted
2 to:
3 interact with the interface to receive the key from said another computer system.

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1 10. An article comprising a storage medium readable by a first processor-
2 based system, the storage medium storing instructions to cause a processor to:
3 receive a key from another processor-based system for identifying the first
4 system,
5 determine whether the key is valid,
6 based on the identification, selectively authorize encryption of an identifier that
7 identifies the first system with the key to produce a hash value.

1 11. The article of claim 10, the storage medium storing instructions to cause
2 the processor to:

3 use an address of said another system to determine whether the key is valid.

1 12. The article of claim 11, wherein the key indicates an URL address.

1 13. The article of claim 10, the storage medium storing instructions to cause
2 the processor to:

3 execute an instruction to cause the processor to subsequently use the key to
4 produce the hash value.

1 14. The article of claim 10, wherein the identifier comprises a processor
2 number.

1 15. A microprocessor comprising:

2 an instruction unit adapted to indicate when the instruction unit receives an
3 instruction that requests an identifier that identifies the microprocessor;

4 an execution unit coupled to the instruction unit and adapted to, in response to the
5 indication from the instruction unit, encrypt a key with the identifier to produce a hash
6 value; and

7 a bus interface unit coupled to the execution unit and adapted to furnish an
8 indication of the hash value to external pins of the microprocessor.

1 16. The microprocessor of claim 15, wherein the execution unit comprises:

2 a control unit coupled to the algorithmic unit and the registers; and

3 a memory coupled to the control unit and storing microcode to cause the control
4 unit to use the key and the identifier to produce the hash value.

1 17. The microprocessor of claim 15, wherein the identifier comprises a
2 processor number.

1 18. The microprocessor of claim 15, wherein the execution unit is adapted to
2 use a one way hash function to produce the hash value.

1 19. The microprocessor claim 15, wherein the execution unit is adapted to use
2 a non-commutative hash function to produce the hash value.

1 20. The microprocessor of claim 15, wherein the execution unit is adapted to
2 use a collision free hash function to produce the hash value.